REMARKS

Claims 1-12 and 38-64 are pending in the present application, were examined, and were rejected. In response, Claims 1 and 7 are amended, no claims are added and no claims are cancelled. Applicants respectfully request reconsideration of pending Claims 1-12 and 38-64 and in view of at least the following remarks.

I. Objections to the Specification

The Examiner has objected to the specification as failing to provide proper antecedent basis for the claimed subject matter. Applicants respectfully traverse the Examiner's objection to the specification.,

In response to the Examiner's objection to the specification, the Examiner respectfully submits that Applicants' specification provides proper support regarding Claims 5, 11, 12 and 40. As indicated in Applicants' specification:

> The decode unit 140 is used for decoding instructions received by computer system 105 into control signals and/or microcode entry points. In response to these control signals and/or microcode entry points, the execution unit 142 performs the appropriate operations. (Pg. 8, lines 10-14.)

As further described by Applicants' specification:

> In one embodiment, the instruction set 165 includes a cache control instruction(s) provided in accordance with the present invention. (Pg. 8, lines 22–24.)

As further described in Applicants' specification:

> Figure 3 illustrates the general operation of the cache control instruction 160 according to one embodiment of the invention. In the practice of the invention, the cache control instruction 160 provides the register (or memory) location which holds a starting address of the data object that the instruction 160 will be operating on. In one embodiment, the starting address includes X most significant bits, which are stored in the register (or memory) location, and Y least significant bits. The cache control process associated with cache control instruction 160, then shifts the X bits to the right by Y positions to obtain the complete starting address. (Pg. 10, lines 17-24.)

Based on the cited passages above, Applicants respectfully submit that one skilled in the art would recognize that cache control instructions during execution within execution unit 142 would perform the described functionality of shifting the X bits to the right by Y positions to obtain the complete starting address, as illustrated in FIG. 3. Accordingly, based on the cited passages above, Applicants respectfully submit that FIG. 3 illustrates a process performed during execution of a cache control instruction within, for example, execution unit 142 in order to provide

antecedent support for Claims 5, 11, 12 and 40. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the objection to the specification for failing to provide proper antecedent basis for the claimed subject matter.

II. Objections to the Drawings under 37 C.F.R. §1.83(a)

The Examiner has objected to the drawings under 37 C.F.R. §1.83(a). Applicants respectfully traverse the Examiner's rejection.

For at least the reasons provided above with respect to the Examiner's objections to the specification, Applicants once again reiterate that one skilled in the art, in view of the cited passages above and FIGS. 1 and 3 of Applicants' specification, would clearly interpret FIG. 3 as illustrating operations performed by execution unit 132 during execution of a cache control instruction. Furthermore, Applicants respectfully submit that requiring the inclusion of execution unit 142, as well as decode unit 140 within FIG. 3, would obscure the details of the invention since the specification clearly illustrates that shifting of the X most significant bits of the starting address by the Y least significant bits in order to provide the start address is clearly illustrated with reference to FIG. 3.

Accordingly, Applicants respectfully submit that Applicants' specification, as filed, provides adequate support for each of the pending claims, including Claims 5, 11, 12 and 40. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the 37 C.F.R. §1.83(a) objection to the drawings.

III. Claims Rejected Under 35 U.S.C. §103

The Patent Office rejects Claims 1-2, 4-12 and 38-64 are rejected under 35 U.S.C. §103(a) as being anticipated by U.S. Patent No. 5,778,431 to Rahman et al. ("Rahman") in view of U.S. Patent No. 5,524,433 to Milburn et al. ("Milburn"). Applicants respectfully traverse this rejection.

To establish a *prima facie* case of obviousness, the following criteria must be met: (1) there must be some suggestion or motivation to modify the reference or combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art references must teach or suggest all the claim limitations. (MPEP §2142) For the reasons provided below, the Examiner has failed to establish a *prima facie* case of obviousness in view of the references of record.

Regarding Claim 1, Claim 1 as amended includes the following claim features, which are neither taught nor suggested by either Rahman, Milburn or the references of record:

> an execution unit coupled to said storage area to operate on data elements in said data operand containing a portion of a user specified starting address to invalidate data in a predetermined portion of the plurality of cache lines beginning at the user specified starting address in response to receiving a single instruction of a processor instruction set. (Emphasis added.)

According to the Examiner, the feature listed above is taught by the combination of Rahman and Milburn. Applicants respectfully disagree with the Examiner's contention based on careful review of Rahman as well as Milburn.

Rahman describes a computer system for selectively invalidating the cache lines of cache memory in response to the removal, modification or disabling of system resources, such as, for example, an external memory. (*See* Abstract.) Based on the background description provided in Rahman, the selective flushing technique of cache memory is provided to eliminate the complete flush of a cache memory any time an external memory device is removed from the system. (*See* col. 2, lines 50-53.)

Rahman describes three techniques for performing selective flushing of cache memory in response to the detection of removal of an external memory card. Within each of the techniques, the external memory card, based on its configuration, provides a certain memory capacity. Accordingly, based on the address range available from the external memory, that address range is compared to tag address values of the cache memory to determine whether a cache line of the cache memory contains data of the external memory. When such is detected, each cache line containing data from the external memory is flushed from the cache memory. (*See* col. 3, lines 10-25.)

As an alternative to the hardware implementation, Rahman describes a microcode implementation to perform a similar process

> As an alternative to his hardware implementation of the present invention, instructions may be written in microcode to perform a similar process. Thus, the start and end address values of the external memory device would be fetched and compared through software routines with the tag address values. An instruction to flush a particular line in the cache memory then would be generated by the process in response to an affirmative comparison. (*See* col. 3, lines 26-33.) (Emphasis added.)

In a further alternative embodiment, a bus interface unit is provided containing an address map of available addresses in the external memory device, which are compared to tag addresses in the cache memory to identify matching tag addresses. Accordingly, each cache line corresponding to matching tagged address is invalidated. (*See* col. 3, lines 26–45.)

Applicants submit that after careful review of the passages cited above, as well as the entire specification of Rahman, Applicants find no teachings or suggestions other than performing of the cache line invalidation and flushing in response to the removal, modification or disabling of an external memory device.

By way of contrast, Claim 1 requires invalidating of data in a predetermined cache memory portion. Conversely, invalidating within Rahman is not based on a predetermined portion. The invalidated portion in Rahman will vary based on the start and address of the external memory and the contents of the cache once the external memory is removed. Furthermore, Claim 1 requires that

the invalidating begins at a user specified starting address. In Rahman, invalidating begins as dictated by the start address of the external memory.

Moreover, Claim 1 requires that the invalidating is performed in response to receiving a single instruction of a processor instruction set. Conversely Rahman performs its invalidation and flushing in response to detected removal of the external memory. Consequently, Applicants submit that the invalidating of the cache lines of a cache memory having data from an external memory, as taught by Rahman, is not performed in response to a single instruction of a processor instruction set, as required by Claim 1.

The Examiner recognizes Rahman's failure to teach a single processor instruction and as a result, cites Milburn. According to the Examiner:

> Milburn shows providing a single instruction with an operation code and address values in its operand (e.g., col. 9, lines 1-10; col. 10, lines 10-15; and col. 11, lines 1-20) are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a single instruction with an operation code and address values in its operand to Rahman's system because it would allow an instruction to influence multiple lines in a cache, invalidating an entire cache range, thereby reducing overall operation times. (Office Action, pg. 4.)

According to the Examiner, the concept and advantages of providing a single instruction with an operation code and address values in its operand are well known and expected in the art. Assuming, *arguendo*, that this proposition is true, the techniques described by Rahman are performed in response to the removal, modification or disabling of system resources. As a result, Applicants submit that one skilled in the art would not perform the selective invalidating using a single instruction of the processor instruction set, since the techniques or instructions to perform such activity are not performed by the direction of a user.

In other words, the techniques described by Rahman are performed without the knowledge of the user and therefore do not need to be made available to the user in the form of a single instruction from the processor instruction set. Accordingly, Applicants submit that one skilled in the art would not perform the selective invalidating of the cache memory of Rahman by providing a single instruction to a user, as required by Claim 1.

Furthermore, Claim 1, as amended, operates according to a user specified starting address, which is contained in an operand of the single instruction of the processor instruction set. By way of contrast, any starting address as taught within Rahman is based on the addresses available in the external memory device. (*See* col. 3, line 36.) Consequently, Applicants submit that the user specified starting address, as required by Claim 1, is neither taught nor suggested by the lower start address register and upper end address register, as taught by Rahman, since such registers are

populated according to the available addresses in the external memory device without any user involvement.

Applicants respectfully submit that the user cannot specify the address ranges within an external memory device, as such parameters are set according to the manufacturing specifications of the external memory device. Accordingly, Applicants respectfully submit that the Examiner has engaged in improper hindsight based analysis in order to render obvious the features of Claim 1, as described above, over Rahman in view of Milburn.

However, the case law is quite clear in establishing that the combination of references cited by an Examiner must teach each and every feature of the claimed invention. The Federal Circuit Court of Appeals in In re Rijckaert, 9 F.3d 1531, 28 U.S.P.Q. 2d 1955 (Fed. Cir. 1993) held that:

> In rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness. . . . "A *prima facie* case of obviousness is established when the teaching from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art.". . . If the examiner fails to establish a *prima facie* case, the rejection is improper and will be overturned. (Emphasis added.) 9 F.3d at 1532, 28 U.S.P.Q. 2d at 1956.

As required by Claim 1, the single instruction, which causes data invalidation in a predetermined portion of the plurality of cache lines beginning at the user specified starting address, in response to receiving a single instruction of a processor instruction set, is not taught nor suggested by either Rahman, Milburn or the references of record. Consequently, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* rejection of Claim 1 as obvious over Rahman in view of Milburn. *Id.* Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 1.

Regarding Claims 4-6, Claims 4-6 depend from Claim 1 and therefore include the patentable claim features of Claim 1, as described above. Therefore, Claims 4-6, for at least the reasons described above, are patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 4–6.

Regarding Claim 7, Claim 7 includes analogous claim features to Claim 1, as described above. Specifically, Claim 7, as amended, includes the following claim features, which are neither taught nor suggested by Rahman, Milburn or the references of record:

> an execution unit coupled to said first storage area, said second storage area, and said cache memory, said execution unit to operate on the portion of a user specified address in said data operand to copy data from a predetermined portion of the plurality of cache lines beginning at the user specified starting address in the cache memory to the first storage area, in response to receiving a single instruction of a processor instruction set. (Emphasis added.)

As indicated above, the teachings of Rahman are limited to selectively invalidating the contents of cache memory upon the detection of the removal, modification or disabling of an external memory device. Accordingly, such selective invalidating of memory is not performed in response to a single instruction of the processor instruction set, as required by Claim 7. Furthermore, the portion from which data is copied from the cache memory is not based on a user specified address, as required by Claim 7. Conversely, the address ranges from which data is invalidated, as taught by Rahman, are based on an available address range of the external memory device and are therefore not user specified, as required by Claim 7.

Accordingly, Applicants submit that the Examiner also fails to establish a *prima facie* rejection of Claim 7 as obvious under §103(a) over Rahman in view of Milburn. Consequently, Applicants respectfully request the Examiner reconsider and withdraw the §103(a) rejection of Claim 7.

Regarding Claims 8-12, Claims 8-12 depend from Claim 7 and therefore include the patentable claim features of Claim 7, as described above. Accordingly, Claims 8-12, for at least the reasons described above, are also patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 8-12.

Regarding Claim 38, Claim 38 includes the following claim feature, which is neither taught nor suggested by either Rahman, Milburn or the references of record:

> an execution unit coupled to said storage area to operate on data elements in said data operand identifying a user-definable linear or physical address identifying a predetermined portion of the plurality of cache lines to invalidate data in the predetermined portion of the plurality of cache lines in response to receiving a single cache control instruction of a processor instruction set, the single cache control instruction including a reference to the data operand.

According to the Examiner, the user-definable linear or physical address is taught by Rahman at col. 3, lines 25-30 and col. 5, lines 30-35 and col. 7, lines 25-28. However, after careful review of the cited passages, Applicants must respectfully disagree with the Examiner's contention. Applicants respectfully submit that careful review of the passages cited by the Examiner establish Applicants' point that the address ranges for which the cache memory contents are invalidated are based on the available addresses of the external memory device; namely:

> the start and end address values of the external memory device would be fetched and compared through software routines with the tag address values. (*See* col. 3, lines 28-31.)
>
> The address tag indicates a physical address in system memory 114 or an external memory (such as may be present, for example, in the removable card driver 144) corresponding to each entry within the cache memory. (*See* col. 5, lines 30-34.)

> In this embodiment, the lower and upper address window values are fetched in a software routine and compared with each of the address tag values fetched from the address tag array. (*See* col. 7, lines 24-27.).

In other words, based on the cited passages, the teachings of Rahman establish start and end addresses, which correspond to available addresses of an external memory device. Such addresses are not user specified. Furthermore, Applicants submit that a user would not be able to modify available addresses provided by an external memory device since configurations of the memory device are based on manufacturing specifications.

Consequently, Applicants submit that the Examiner cannot establish a *prima facie* rejection of Claim 38 over Rahman in view of Milburn since the combination of references fails to teach a user-definable linear or physical address identifying a portion of the plurality of cache links to invalidate in response to a single cache control instruction, as required by Claim 38. *Id.* Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 38.

Regarding Claims 39-41, Claims 39-41 depend from Claim 38 and therefore include the patentable claim features of Claim 38, as described above. Accordingly, Claims 39-41, for at least the reasons described above, are also patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 39-41.

Regarding Claim 42, Claim 42 includes the following claim feature, which is neither taught nor suggested by either Rahman, Milburn or the references of record:

> read a portion of an address located in a register specified in the decoded instruction to obtain a user specified starting address of a predetermined area of a cache memory on which the instruction will be performed; and invalidate in the predetermined area of cache memory. (Emphasis added.)

As indicated above, both Rahman and Milburn fail to teach or suggest a user specified starting address within which to invalidate cache memory data. As indicated above, the area in which cache memory is invalidated is based on the address range available of an external memory card. Furthermore, neither Rahman, Milburn or the references of record fail to teach invalidation performed in response to a single decoded instruction.

Accordingly, for at least the reasons described above, Applicants respectfully submit that the Examiner has failed to establish and cannot establish a *prima facie* rejection of Claim 42 since case law clearly requires that the combination of references must teach or suggest each and every claim limitation, as required by Claim 42. *Id.* Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 42.

Regarding Claims 43-45, Claims 43-45 depend from Claim 42 and therefore include the patentable claims features of Claim 42, as described above. Accordingly, Claims 43-45, for at

least the reasons described above, are patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 43–45.

Regarding Claim 46, Claim 46 includes the following claim feature, which is neither taught nor suggested by Rahman, Milburn or the references of record:

> a circuit coupled to said decoder, said circuit in response to a single decoded instruction of a processor instruction set being configured to: read a portion of an address located in a register specified in the decoded instruction to obtain a user specified starting address of a predetermined area of a cache memory on which the instruction will be performed. (Emphasis added.)

As indicated above, the area in which invalidation is performed as taught by Rahman is based on the memory range or memory capacity of an external memory card, which may not be user specified. Furthermore, the techniques performed by Rahman are not performed in response to a processor instruction set instruction. Applicants submit that one skilled in the art would not modify Rahman to implement selective invalidating of the cache memory in response to a single processor instruction set instruction since such activity is performed internally within the processor when modification, disabling or removal of system resources, and specifically removal of an external memory device, is detected.

Accordingly, for at least the reasons described above, Applicants submit that the Examiner cannot establish a *prima facie* rejection of Claim 46 under 35 U.S.C. §103(a) over Rahman in view of Milburn since the combination of references of fails to teach or suggest every claim feature of Claim 46, as described above. *Id.* Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 46.

Regarding Claims 47-50, Claims 47-50 depend from Claim 46 and therefore include the patentable claim features of Claim 46. Accordingly, for at least the reasons described above, Claims 47-50 are patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 47-50.

Regarding Claims 51 and 62, Claims 51 and 62 include the following claim features, which are neither taught nor suggested by the references of record:

> in response to said decoding of the single instruction, obtaining a portion of a user specified starting address of a predetermined area of a cache memory on which the single instruction will be performed by reading a portion of an address contained in a storage location specified in the decoded instruction. (Emphasis added.)

As indicated above, the starting address referred to within Rahman refers to the start address of an available memory range or capacity of an external memory device. As indicated, the capacity and address range of the external memory device may not be modified by a user and is therefore not user specified, as required by Claim 51. Furthermore, neither Rahman nor Milburn

teach the invalidating of data within the predetermined portion of memory in response to a single instruction.

As indicated, the invalidating, as described by Rahman, is performed internally within the computer in response to modification, disabling or removal of system resources and specifically, the external memory device. Moreover, Rahman does not describe a predetermined area in which invalidating is performed. The area in which invalidating is performed within Rahman is based on the address range or memory capacity of the external memory device.

Accordingly, for at least the reasons described above, Applicants respectfully submit that the Examiner cannot establish a *prima facie* rejection of Claims 51 and 62 under 35 U.S.C. §103(a) as obvious over Rahman in view of Milburn since the combination of references fails to teach or suggest each and every claim limitation of Claims 51 and 62. *Id.* Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 51 and 62.

Regarding Claims 52-55, Claims 52-55 depend from Claim 51 and therefore include the patentable claim features of Claim 51, as described above. Accordingly, Claims 52-55, for at least the reasons described above, are also patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 52-55.

Regarding Claims 56 and 63, Claims 56 and 63 include the following claim feature, which is neither taught nor suggested by the references of record:

> in response to said decoding the single instruction, obtaining a portion of a user specified starting address of a predetermined area of a cache memory on which the single instruction will be performed by reading a portion of an address contained in a storage location specified in the decoded instruction. (Emphasis added.)

As indicated, the starting address within which invalidating is performed within Rahman cannot be user specified since the starting address is based on the address range or memory capacity of the external memory device. Furthermore, the teachings of Rahman for the invalidating are not performed in response to a single processor instruction set instruction since such techniques are performed internally within the processor and therefore do not require availability to a system programmer. Moreover, the predetermined area of cache memory is not taught by Rahman since the area of cache memory for invalidating is based on the address range or memory capacity via external memory device.

Accordingly, for at least the reasons described above, Applicants respectfully submit that the Examiner cannot establish a *prima facie* rejection of Claims 56 and 63 under 35 U.S.C. §103(a) as obvious over Rahman in view of Milburn since the combination of references fail to teach the claim features of Claims 56 and 63, as described above. *Id.* Consequently, Applicants

respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 56 and 63.

Regarding Claims 57-61, Claims 57-61 depend from Claim 56 and therefore include the patentable claim features of Claim 56, as described above. Accordingly, for at least the reasons described above, Claims 57-61 are also patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 57-61.

Regarding Claim 64, Claim 64 depends from Claim 63 and therefore includes the patentable claim features of Claim 63. Accordingly, Claim 64, for at least the reasons described above, is also patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 64.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: February 17, 2004

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. 1450, Alexandria, VA 22313-1450 on February 17, 2004

Marilyn Bass February 17, 2004